WHAT IS CLAIMED IS:

1. A semiconductor memory having a memory cell array region and peripheral circuit region, comprising:

a gate electrode formed on a semiconductor substrate via an insulating film in each of said memory cell array region and peripheral circuit region, and including a conductive layer;

a first oxide film formed on side surfaces of said conductive layer of said gate electrode and on said semiconductor substrate in said memory cell array region;

a second oxide film formed on side surfaces of said conductive layer of said gate electrode and on said semiconductor substrate in said peripheral circuit region, and having a film thickness smaller than that of said first oxide film;

a first nitride film formed on side surfaces of said gate electrode in said memory cell array region; and

a second nitride film formed on side surfaces of said gate electrode in said peripheral circuit region, and having a film thickness larger than that of said first nitride film.

2. A memory according to claim 1, wherein a bird's beak formed by said first oxide film below the side surface of said gate electrode in said memory cell array region is larger than a bird's beak formed by said second oxide film below the side surface of said gate electrode in said peripheral circuit region.

3. A memory according to claim 1, further comprising:

in said peripheral circuit region, first source and drain diffusion layers formed by implanting an impurity into a surface portion of said semiconductor substrate by using, as masks, said gate electrode and said second oxide film on the side surfaces of said conductive layer included in said gate electrode; and in said memory cell array region, second source and drain diffusion layers formed by implanting an impurity into a surface portion of said semiconductor substrate by using, as masks, said gate electrode and said first oxide film on the side surfaces of said conductive layer included in said gate electrode.

4. A memory according to claim 1, further comprising:

in said peripheral circuit region, third source and drain diffusion layers formed by implanting an impurity into a surface portion of said semiconductor substrate by using, as masks, said gate electrode, said second oxide film on the side surfaces of said conductive layer included in said gate electrode, and said second nitride film formed on the side surfaces of said gate electrode; and

in said memory cell array region, fourth source and drain diffusion layers formed by implanting an impurity into a surface portion of said semiconductor substrate by using, as masks, said gate electrode, said first oxide film on the side surfaces of said conductive layer included in said gate electrode, and said first nitride film formed on the side surfaces of said gate electrode.

5. A semiconductor memory having a memory cell array region and peripheral circuit region, comprising:

a gate electrode formed on a semiconductor substrate via an insulating film in each of said memory cell array region and peripheral circuit region;

a first oxide film formed on side surfaces of said gate electrode in said memory cell array region;

a second oxide film formed on side surfaces of said gate electrode in said peripheral circuit region, and having a film thickness smaller than that of said first oxide film;

a first nitride film formed on said first oxide film on the side surfaces of said gate electrode in said memory cell array region; and a second nitride film formed on said second oxide film on the side surfaces of said gate electrode in said peripheral circuit region, and having a film thickness larger than that of said first nitride film.

6. A memory according to claim 1, further comprising a trench capacitor formed in a surface portion of said semiconductor substrate in said memory cell array region.

7. A memory according to claim 1, further comprising a stacked capacitor formed above said semiconductor substrate in said memory cell array region.

8. A method of manufacturing a semiconductor memory having a memory cell array region and peripheral circuit region, comprising:

forming a first insulating film on a semiconductor substrate in the memory cell array region and peripheral circuit region;

forming, on the first insulating film, a conductive layer which at least partially includes a silicon layer, and a second insulating film;

forming a gate electrode by patterning the conductive layer and second insulating film into a gate electrode shape;

forming a first oxide film by annealing side surfaces of the conductive layer included in the gate electrode and a surface of the semiconductor substrate in an oxidizing ambient;

forming a first nitride film on an entire surface;

patterning the first nitride film such that the first nitride film is removed from the memory cell array region and left behind in the peripheral circuit region;

forming a second oxide film by annealing side surfaces of the conductive layer included in the gate electrode and a surface of the semiconductor substrate in the memory cell array region in an oxidizing ambient, while the peripheral circuit region is covered with the first nitride film;

etching the first nitride film remaining in the peripheral circuit region to leave the first nitride film behind on side surfaces of the gate electrode in the peripheral circuit region;

forming a second nitride film on an entire surface; and

etching the second nitride film to leave the second nitride film behind on the side surfaces of the gate electrodes in the memory cell array region and peripheral circuit region.

9. A method according to claim 8, further comprising:

forming, in the peripheral circuit region, first source and drain diffusion layers by implanting an impurity into a surface portion of the semiconductor substrate by using, as masks, the gate electrode, and the first oxide film on the side surfaces of the conductive layer included in the gate electrode; and

forming, in the memory cell array region, second source and drain diffusion layers by implanting an impurity into a surface portion of the semiconductor substrate by using, as masks, the gate electrode, and the first and second oxide films on the side surfaces of the conductive layer included in the gate electrode.

10. A method according to claim 9, further comprising:

forming, in the peripheral circuit region, third source and drain diffusion layers by implanting an impurity into the surface portion of the semiconductor substrate by using, as masks, the gate electrode, the first oxide film on the side surfaces of the conductive layer included in the gate electrode, and the first and second nitride films formed on the side surfaces of the gate electrode; and

forming, in the memory cell array region, fourth source and drain diffusion layers by implanting an impurity into the surface portion of the semiconductor substrate by using, as masks, the gate electrode, the first and second oxide films on the side surfaces of the conductive layer included in the gate electrode, and the second nitride film formed on the side surfaces of the gate electrode.

11. A method according to claim 9, further comprising:

forming, in the peripheral circuit region, fifth source and drain diffusion layers by implanting an impurity into the surface portion of the semiconductor substrate by using, as masks, the gate electrode, the first oxide film on the side surfaces of the conductive layer included in the gate electrode, and the first nitride film formed on the side surfaces of the gate electrode;

forming, in the peripheral circuit region, sixth source and drain diffusion layers by implanting an impurity into the surface portion of the semiconductor substrate by using, as masks, the gate electrode, the first oxide film on the side surfaces of the conductive layer included in the gate electrode, and the first and second nitride films formed on the side surfaces of the gate electrode; and

forming, in the memory cell array region, seventh source and drain diffusion layers by implanting an impurity into the surface portion of the semiconductor substrate by using, as masks, the gate electrode, the first and second oxide films on the side surfaces of the conductive layer included in the gate electrode, and the second nitride film formed on the side surfaces of the gate electrode.

12. A method of manufacturing a semiconductor memory having a memory cell array region and peripheral circuit region, comprising:

forming a first insulating film on a semiconductor substrate in the memory cell array region and peripheral circuit region;

forming a conductive layer which at least partially includes a silicon layer on the first insulating film;

forming a gate electrode by patterning the conductive layer into a gate electrode shape;

forming a first oxide film by annealing side surfaces of the gate electrode and a surface of the semiconductor substrate in an oxidizing ambient;

forming a first nitride film on an entire surface;

patterning the first nitride film such that the first nitride film is removed from the memory cell array region and left behind in the peripheral circuit region;

forming a second oxide film by annealing the side surfaces of the gate electrode and the surface of the semiconductor substrate in the memory cell array region in an oxidizing ambient, while the peripheral circuit region is covered with the first nitride film;

etching the first nitride film remaining in the peripheral circuit region to leave the first nitride film behind on the side surfaces of the gate electrode in the peripheral circuit region;

forming a second nitride film on an entire surface; and

etching the second nitride film to leave the second nitride film behind on the side surfaces of the gate electrodes in the memory cell array region and peripheral circuit region.

13. A method according to claim 12, further comprising:

forming, in the peripheral circuit region, first source and drain diffusion layers by implanting an impurity into a surface portion of the semiconductor substrate by using, as masks, the gate electrode, and the first oxide film on the side surfaces of the gate electrode; and

forming, in the memory cell array region, second source and drain diffusion layers by implanting an impurity into a surface portion of the semiconductor substrate by using, as masks, the gate electrode, and the first and second oxide films on the side surfaces of the gate electrode.

14. A method according to claim 13, further comprising:

forming, in the peripheral circuit region, third source and drain diffusion layers by implanting an impurity into the surface portion of the semiconductor substrate by using, as masks, the gate electrode, the first oxide film on the side surfaces of the gate electrode, and the first and second nitride films formed on the side surfaces of the gate electrode; and

forming, in the memory cell array region, fourth source and drain diffusion layers by implanting an impurity into the surface portion of the semiconductor substrate by using, as masks, the gate electrode, the first and second oxide films on the side surfaces of the gate electrode, and the second nitride film formed on the side surfaces of the gate electrode.

15. A method according to claim 13, further comprising:

in the peripheral circuit region, exposing a surface of the conductive layer of the gate electrode having the first and second nitride films formed on the side surfaces, by removing the first oxide film from the surface of the conductive layer, and exposing a surface of the semiconductor substrate in a region where the gate electrode is not formed, by removing the first insulating film and the first oxide film from the surface of the semiconductor substrate, and, in the memory cell array region, exposing a surface of the conductive layer of the gate electrode having the second nitride film formed on the side surfaces, by removing the first and second oxide films from the surface of the conductive layer, and exposing a surface of the semiconductor substrate in a region where the gate electrode is not formed, by removing the first insulating film and the first and second oxide films from the surface of the semiconductor substrate;

forming a metal film on an entire surface; and

annealing, in the peripheral circuit region, the metal film present on the gate electrode having the exposed surface, and on the semiconductor substrate having the exposed surface in the region where the gate electrode is not formed, and, in the memory cell array region, the metal film present on the gate electrode having the exposed surface, and on the semiconductor substrate having the exposed surface in the region where the gate electrode is not formed, thereby forming a metal silicon compound film.

16. A method according to claim 8, further comprising a step of forming a trench capacitor in the surface portion of the semiconductor substrate in the memory cell array region.

17. A method according to claim 8, further comprising a step of forming a stacked capacitor above the semiconductor substrate in the memory cell array region.